ABSTRACT OF THE DISCLOSURE

A semiconductor device having at least three independently accessible memories, with at least one of the memories having a different memory capacity than the others. Separate selection signals are provided to the memories so that they can be independently activated. This allows the memories to be separately tested. When testing the semiconductor device, the memories are tested serially, except for the memory with the largest capacity, since this memory also has the longest test time. The memory with the longest test time is tested in parallel with the serially tested memories. This reduces the current that must be supplied by a test device to the semiconductor device during testing.